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COUGHLAN, PETER D	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,050	SALAM ET AL.	
	Examiner	Art Unit	
	PETER COUGHLAN	2129	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *43-48,51-67 and 70-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *43-48,51-67 and 70-88* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/5/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to an AMENDMENT entered June 17, 2008 for the patent application 10/773050 filed on February 5, 2004.

2. All previous Office Actions are fully incorporated into this Final Office Action by reference.

3. Examiner's Comment: Although, the terms 'carrier wave' or 'carrier signal' is not specifically mentioned within the specification, the Examiner will exclude these interpretations wherein the context of 'storage medium' is disclosed.

Status of Claims

4. Claims 43-48, 51-67, 70-88 are pending.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 43, 62, 81 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. These amended claims state 'a digital memory arranged in parallel with the capacitor and operable to store the local weight in a digital form.' This is contrary to the specification, ¶0040 which states 'For example, on-chip storage may be accomplished in the analog domain with capacitors while learning may be accomplished in the digital domain.' The specification states the weights are stored in analog with a capacitor, and learning is accomplished by digital means. The specification does not state that the local weights are stored within a capacitor in a digital form. These claims need to follow the specification description of the invention.

These claims need to be amended or withdrawn from consideration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

Claims 43-48, 51-57, 59-67, 70-76, 78-88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh, in view of Schwartz. ('Analog CMOS implementation of artificial neural networks for temporal signal learning', referred to as **Oh**; 'A programmable analog neural network chip', referred to as **Schwartz**)

Claim 43

Oh teaches an array of synaptic cells, which are interconnected to form a feedforward neural network, wherein each synaptic cell includes. (**Oh**, p4:19 through p5:2)

Oh does not teach a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor in the cell, a digital memory operable to store the local weight in a digital form.

Schwartz teaches a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor in the cell, a digital memory arranged in parallel with the capacitor and operable to store the local weight in a digital form. (**Schwartz**, abstract, p313 C1:1 through p314 C1:27 'Learning electrical circuit operable to update a local weight according to an update rule' of applicant is equivalent to 'neural network' of Schwartz. 'A digital memory arranged in parallel with the capacitor and operable to store the local weight in a digital form' of applicant is equivalent to 'Our experiments show that careful designs can reduce leakage to a level

low enough that analog refresh by backing up the network with the conventional analog/digital conversion techniques and digital memory is practical if desired' of Schwartz. 'Arranged in parallel' of applicant is equivalent to 'parallel computing' of Schwartz.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Oh by using both analog and digital storage devices as taught by Schwartz to have a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor in the cell, a digital memory operable to store the local weight in a digital form.

For the purpose of having low hardware overhead for learning.

Oh teaches a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of an analog input signal in accordance with the local weight stored in the digital memory.(**Oh**, abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.)

Claim 44

Oh teaches wherein each column of synaptic cells in the array of synaptic cells represents a neuron in the neural network. (**Oh**, Figure 6.2; One function of a neuron is to use its output for training to convergence. The column(s) of Figure 6.2 illustrate this by using the outcome of 'error' circuit for training purposes.)

Claim 45

Oh teaches an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a row of synaptic cells in the array of synaptic cells. (**Oh**, p116:2-17; Oh discloses an analog to digital converter to have analog input stored in digital form.)

Claim 46

Oh teaches wherein the control cells operate synchronously with each other to control conversion. (**Oh**, p12:14 through p13:3; Oh discloses in the McCulloch-Pitts model, in which neurons operate in asynchronous manner. Using Oh's model in which the feedforward neural network is interconnected allows synchronously operations to Occur.)

Claim 47

Oh teaches wherein each control cell includes a multiplexer configured to select a synaptic cell in a given row of synaptic cells (**Oh**, figure 6.2; Figure 6.2 illustrates numerous multiplexers within the recurrent neural network.) and an analog-to-digital converter. (**Oh**, pl 16:2-17)

Claim 48

Oh teaches wherein the analog-to-digital converter for a given row of synaptic cells is interconnected to each synaptic cell in the given row of synaptic cells. (**Oh**, p116:2-17)

Claim 51

Oh teaches a switch interposed between the processing circuit and the digital memory for selectively enabling use of the digital memory. (**Oh**, p116:2-17; Oh discloses a second recurrent neural network (slave neural network) which employs the weight values from the first recurrent neural network. These values are updated using the digital memory. If a user can alter between the first and second recurrent neural network, then there exists a 'switch' to do so.)

Claim 52

Oh teaches a switch interposed between the processing circuit and the learning circuit for selectively enabling use of the learning circuit. (**Oh**, p116:2-17; Oh discloses a first recurrent neural network (master neural network) which employs the learning phase of the neural network or learning circuit of applicant. These values are updated using the digital memory. If a user can alter between the first and second recurrent neural network, then there exists a 'switch' to do so.)

Claim 53

Oh teaches a switch interposed between the processing circuit, the learning circuit and the digital memory for selectively enabling the use of either the learning circuit or the digital memory by the processing circuit. (**Oh**, p116, 2-17; If there exists two phases, a learning phase and a testing phase, then there exists a switch to alter between the two phases.)

Claim 54

Oh teaches the learning circuit is comprised of a one-dimensional multiplier for implementing the update rule. (**Oh**, abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.)

Claim 55

Oh teaches the learning circuit is configured to receive an error signal indicative of a difference between an output signal and a target output signal. (**Oh**, p15:9 through p16:7; 'Output signal' and 'target output signal' of applicant is equivalent to 'actual output' and 'desired output' of Oh.)

Claim 56

Oh teaches multiple arrays of synaptic cells, which are interconnected to form a multi-layer neural network. (**Oh**, figure 6.2; Figure 6.2; The 2 dimensional array which each node is interconnected with other nodes of Oh is equivalent to 'multi-layer neural network' of applicant.)

Claim 57

Oh teaches the learning circuit further comprises a second multiplier configured to receive the error signal and generates a feedback propagation error signal for a previous layer in the multi-layer neural network.(**Oh**, p17:5-6 and equation (2.11); 'Error signal' of applicant is equivalent to 'wk' of Oh. 'Previous layer' of applicant is equivalent to 'W^{k-1}' of Oh.)

Claim 59

Oh teaches a digital-to-analog converter interposed between the processing circuit and the digital memory in each synaptic cell. (**Oh**, p116:2-17; Oh discloses a digital to analog converter for outputting the value of the synaptic cell.)

Claim 60

Oh teaches wherein each processing circuit in a column of synaptic cells outputs a component of a weighted sum. (**Oh**, p13:4 through p15:8; 'Processing circuit in a column' of applicant is equivalent to 'the 'hidden layer' of Oh. 'Outputs a component of a weighted sum' of applicant is equivalent to the output of each node in the hidden layer is a result of the weighted sum input.)

Claim 61

Oh teaches wherein an output of each multiplier in a column of synaptic cells is interconnected to form a weighted sum. (**Oh**, figure 5.5; Oh discloses the output of each multiplier (Y_1-Y_4) is fed back as a column to form an interconnection of synaptic cells.)

Claim 62

Oh teaches an array of synaptic cells which are interconnected to form a feedforward neural network (**Oh**, p4:19 through p5:2) and configured to receive an analog input signal indicative of a biological cell measurement and to model a process of the biological cell, wherein each synaptic cell includes (**Oh**, p3:6-10; 'Configured to receive ... analog input' of applicant is disclosed by a 'subthreshold analog CMOS VLSI' of Oh .)

Oh does not teach a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor in the cell, a digital memory arranged in parallel with the capacitor and operable to store the local weight in a digital form.

Schwartz teaches a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor in the cell, a digital memory arranged in parallel with the capacitor and operable to store the local weight in a digital form. (**Schwartz**, abstract, p313 C1:1 through p314 C1:27 'Learning electrical circuit operable to update a local weight according to an update rule' of applicant is equivalent to 'neural network' of Schwartz. 'A digital memory arranged in parallel with the capacitor and operable to store the local weight in a digital form' of applicant is

equivalent to ‘Our experiments show that careful designs can reduce leakage to a level low enough that analog refresh by backing up the network with the conventional analog/digital conversion techniques and digital memory is practical if desired’ of Schwartz. ‘Arranged in parallel’ of applicant is equivalent to ‘parallel computing’ of Schwartz.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Oh by using both digital and analog storage devices as taught by Schwartz to have a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor in the cell, a digital memory in the cell operable to store the local weight in a digital form.

For the purpose of having low hardware overhead for learning.

Oh teaches a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of the analog input signal in accordance with the local weight stored in the digital memory. (**O**h, abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.)

Claim 63

Oh teaches wherein each column of synaptic cells in the array of synaptic cells represents a neuron in the neural network. (**Oh**, Figure 6.2; One function of a neuron is to use its output for training to convergence. The column(s) of Figure 6.2 illustrate this by using the outcome of 'error' circuit for training purposes.)

Claim 64

Oh teaches an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a row of synaptic cells in the array of synaptic cells. (**Oh**, p116:2-17; Oh discloses an analog to digital converter to have analog input stored in digital form.)

Claim 65

Oh teaches wherein the control cells operate synchronously with each other to control conversion. (**Oh**, p12:14 through p13:3; Oh discloses in the McCulloch-Pitts model, in which neurons operate in asynchronous manner. Using Oh's model in which the feedforward neural network is interconnected allows synchronously operations to Occur.)

Claim 66

Oh teaches wherein each control cell includes a multiplexer configured to select a synaptic cell in a given row of synaptic cells (**O**h, figure 6.2; Figure 6.2 illustrates numerous multiplexers within the recurrent neural network.) and an analog-to-digital converter. (**Oh**, pl 16:2-17)

Claim 67

Oh teaches wherein the analog-to-digital converter for a given row of synaptic cells is interconnected to each synaptic cell in the given row of synaptic cells. (**Oh**, p116:2-17)

Claim 70

Oh teaches a switch interposed between the processing circuit and the digital memory for selectively enabling use of the digital memory. (**Oh**, p116:2-17; Oh discloses a second recurrent neural network (slave neural network) which employs the weight values from the first recurrent neural network. These values are updated using the digital memory. If a user can alter between the first and second recurrent neural network, then there exists a 'switch' to do so.)

Claim 71

Oh teaches a switch interposed between the processing circuit and the learning circuit for selectively enabling use of the learning circuit. (**Oh**, p116:2-17; Oh discloses a first recurrent neural network (master neural network) which employs the learning phase of the neural network or learning circuit of applicant. These values are updated using the digital memory. If a user can alter between the first and second recurrent neural network, then there exists a 'switch' to do so.)

Claim 72

Oh teaches a switch interposed between the processing circuit, the learning circuit and the digital memory for selectively enabling the use of either the learning circuit or the digital memory by the processing circuit. (**Oh**, p116, 2-17; If there exists two phases, a learning phase and a testing phase, then there exists a switch to alter between the two phases.)

Claim 73

Oh teaches the learning circuit is comprised of a one-dimensional multiplier for implementing the update rule. (**Oh**, abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.)

Claim 74

Oh teaches the learning circuit is configured to receive an error signal indicative of a difference between an output signal and a target output signal. (**Oh**, p15:9 through p16:7; 'Output signal' and 'target output signal' of applicant is equivalent to 'actual output' and 'desired output' of Oh.)

Claim 75

Oh teaches multiple arrays of synaptic cells, which are interconnected to form a multi-layer neural network. (**Oh**, figure 6.2; Figure 6.2; The 2 dimensional array which each node is interconnected with other nodes of Oh is equivalent to 'multi-layer neural network' of applicant.)

Claim 76

Oh teaches the learning circuit further comprises a second multiplier configured to receive the error signal and generates a feedback propagation error signal for a previous layer in the multi-layer neural network.(**Oh**, p17:5-6 and equation (2.11); 'Error signal' of applicant is equivalent to 'wk' of Oh. 'Previous layer' of applicant is equivalent to 'W^{k-1}' of Oh.)

Claim 78

Oh teaches a digital-to-analog converter interposed between the processing circuit and the digital memory in each synaptic cell. (**Oh**, p116:2-17; Oh discloses a digital to analog converter for outputting the value of the synaptic cell.)

Claim 79

Oh teaches wherein each processing circuit in a column of synaptic cells outputs a component of a weighted sum. (**Oh**, p13:4 through p15:8; 'Processing circuit in a column' of applicant is equivalent to 'the 'hidden layer' of Oh. 'Outputs a component of a weighted sum' of applicant is equivalent to the output of each node in the hidden layer is a result of the weighted sum input.)

Claim 80

Oh teaches wherein an output of each multiplier in a column of synaptic cells is interconnected to form a weighted sum. (**Oh**, figure 5.5; Oh discloses the output of each multiplier (Y_1-Y_4) is fed back as a column to form an interconnection of synaptic cells.)

Claim 81

Oh teaches an array of synaptic cells which are interconnected to form a feedforward neural network (**Oh**, p4:19 through p5:2), wherein each synaptic cell includes: a learning circuit (**Oh,** p4:19-25; 'Learning circuit' of applicant is equivalent to 'learning circuit' of Oh.) operable to update a local weight (**Oh,** p4:19-25; 'Updating a local weight' of applicant is disclosed by the ability of the first neural network to fed the second neural network of Oh.) according to an update rule (**Oh,** p20 through p22; 'Update rule' of applicant is equivalent to 'modified update law' of Oh.) and store the local weight in a capacitor (**Oh,** p4:10-18; ' Store the local weight in a capacitor' of applicant is disclosed by 'adjustable analog weights … storage technique … across a capacitor' of Oh.) wherein the learning circuit is comprised of a one-dimensional multiplier for implementing the update rule (Oh, abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.), and is configured to receive an error signal indicative of a difference between an output signal and a target output signal. (**Oh**, p15:9 through p16:7; 'Output signal' and 'target output signal' of applicant is equivalent to 'actual output' and 'desired output' of Oh.)

Oh does not teach a digital memory operable to store the local weight in a digital form.

Schwartz teaches a digital memory arranged in parallel with the capacitor and operable to store the local weight in a digital form. (**Schwartz**, abstract, p313 C1:1 through p314 C1:27 'Learning electrical circuit operable to update a local weight according to an update rule' of applicant is equivalent to 'neural network' of Schwartz. 'A digital memory arranged in parallel with the capacitor and operable to store the local weight in a digital form' of applicant is equivalent to 'Our experiments show that careful designs can reduce leakage to a level low enough that analog refresh by backing up the network with the conventional analog/digital conversion techniques and digital memory is practical if desired' of Schwartz. 'Arranged in parallel' of applicant is equivalent to 'parallel computing' of Schwartz.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Oh by using digital memory as taught by Schwartz to have a digital memory arranged in parallel with the capacitor and operable to store the local weight in a digital form.

For the purpose of having a stable source of reliable information without concerns of capacitor storage accuracy.

Oh and Schwartz do not teach wherein the digital memory is implemented using flip-flops.

Newton teaches wherein the digital memory is implemented using flip-flops. (**Newton**, p316, C2:43-45; It is common knowledge that a flip flop circuit is used to hold digital information.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the combined teachings of Oh and

Schwartz by using flip flops as taught by Newton to have wherein the digital memory is implemented using flip-flops.

For the purpose of using established circuit design for reliable results.

Oh teaches a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of an analog input signal in accordance with the local weight stored in the digital memory (**Oh**, abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.) a switch interposed between the processing circuit, the learning circuit, and the digital memory for selectively enabling the use of either the learning circuit or the digital memory by the processing circuit (**Oh**, p116, 2-17; If there exists two phases, a learning phase and a testing phase, then there exists a switch to alter between the two phases.); a digital-to-analog converter interposed between the processing circuit and the digital memory in each synaptic cell. (**Oh**, p116:2-17)

Claim 82

Oh teaches multiple arrays of synaptic cells which are interconnected to form a multi-layer neural network (**Oh**, figure 6.2; Figure 6.2; The 2 dimensional array which each node is interconnected with other nodes of Oh is equivalent to 'multi-layer neural network' of applicant.), wherein the learning circuit further comprises a second multiplier configured to receive the error signal and generates a feedback propagation error signal for a previous layer in the multi-layer neural network. (**Oh**, p17:5-6 and equation (2.11);

'Error signal' of applicant is equivalent to 'w^k' of Oh. 'Previous layer' of applicant is equivalent to 'w^{k-1}' of Oh.)

Claim 83

Oh teaches an output of each multiplier in a column of synaptic cells is interconnected to form a weighted sum, and each processing circuit in a column of synaptic cells outputs a component of the weighted sum. (**Oh**, figure 5.5; Oh discloses the output of each multiplier (Y_1-Y_4) is a result of the summation of weights for a given row. The output of each multiplier is returned into the interconnected array as a column.)

Claim 84

Oh teaches wherein each column of synaptic cells in the array of synaptic cells represents a neuron in the neural network. (**Oh**, Figure 6.2; One function of a neuron is to use its output for training to convergence. The column(s) of Figure 6.2 illustrate this by using the outcome of 'error' circuit for training purposes.)

Claim 85

Oh teaches an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a row of synaptic cells in the array of synaptic cells. (**Oh**,

p116:2-17; Oh discloses an analog to digital converter to have analog input stored in digital form.)

Claim 86

Oh teaches wherein the control cells operate synchronously with each other to control conversion. (**Oh**, p12:14 through p13:3; Oh discloses in the McCulloch-Pitts model, in which neurons operate in asynchronous manner. Using Oh's model in which the feedforward neural network is interconnected allows synchronously operations to Occur.)

Claim 87

Oh teaches wherein each control cell includes a multiplexer configured to select a synaptic cell in a given row of synaptic cells (Oh, figure 6.2; Figure 6.2 illustrates numerous multiplexers within the recurrent neural network.) and an analog-to-digital converter. (**Oh**, pl 16:2-17)

Claim 88

Oh teaches wherein the analog-to-digital converter for a given row of synaptic cells is interconnected to each synaptic cell in the given row of synaptic cells. (**Oh**, p116:2-17)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 58, 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Oh and Schwartz as set forth above, in view of Newton. ('Newton's Telecom Dictionary', referred to as Newton)

Claims 58, 77

Oh and Schwartz do not teach wherein the digital memory is implemented using flip-flops.

Newton teaches wherein the digital memory is implemented using flip-flops. (**Newton**, p316, C2:43-45; It is common knowledge that a flip flop circuit is used to hold digital information.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Oh and Schwartz by disclosing the flip flop circuit as taught by Newton to have the digital memory is implemented using flip-flops.

For the purpose of using industrial standard technology for containing digital values.

Response to Arguments

6. Applicant's arguments filed on June 17, 2008 for claims 43-48, 51-67, 70-88 have been fully considered but are not persuasive.

7. In reference to the Applicant's argument:

REMARKS

Claims 43-48, 51-67 and 70-88 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 103

Claims 43-48, 51-57, 59-67, 70-76 and 78-80 stand rejected under 35 U.S.C. §102(b) as being unpatentable over a dissertation by Oh entitled "Analog CMOS Implementation of Artificial Neural Networks for Temporal Signal Learning" (Oh) in view of article by Lehmann et al entitled "MixedAnalog/Digital Matrix-Vector Multiplier for Neural Network Synapses" (Lehmann). This rejection is respectfully traversed.

Oh relates generally to an analog implementation of an artificial neural network. As conceded by the Examiner, Oh does not teach a learning circuit that updates a local weight and stores the local weight in a capacitor as well as in a digital memory within the cell. The Examiner relies upon Lehmann to teach this aspect of the present invention.

Lehmann relates generally to a mixed matrix-vector multiplier for neural networks. Of note, Lehmann suggests the use of a capacitor as an "analog extension" to a digital memory. This means that the analog capacitor will accumulate the difference between what the digital memory is storing and what a learning method may need the value to be (i.e., it computes a differential and then uses a counter to increment the digital memory). Such an "analog extension" has no operability support or justification. There is no supportive engineering analysis that ensures this method would work and it is highly likely that it will face serious stability issues. Lehmann further assumes that a learning method would be able to do that without any considerations that the learning method will encounter instability. It is noteworthy that Lehmann does not provide any specific teachings for how learning would be implemented but merely outlines an approach. Thus, how learning is implemented in hardware is in fact speculative and open to questions including instability. Thus, this combination of references does not yield a predictable result. KSR International Co. v. Teleflex Inc. 82 USPQ2d 1385 (2007). In addition, the proposed modification by the Examiner cannot render the teachings of Oh unsatisfactory for its intended purpose nor can it change the principle of operation. See, MPEP 2143.01. For these reasons, applicant contends that the teachings of Lehmann cannot be combined with Oh.

Furthermore, the use of a capacitor as an "analog extension" means that the capacitor in Lehmann is in the same path or in series with the digital memory, thereby creating a mixed-mode arrangement. In contrast, applicant's invention discloses a cell arrangement where a capacitor is arranged in parallel with a digital memory. In this way, applicant's invention implements learning methods entirely in an analog domain, thereby avoiding the mixed mode issues (i.e., non-convergence) associated with Lehmann. Pending claims have been amended to clarify this aspect of the present invention. Basis for this amendment may be found throughout the application as originally filed, including Figure 2. For this additional reason, the pending claims define patentably subject matter over the relied upon combination of references. Accordingly, Applicants respectfully request the Examiner reconsider and withdraw these rejections.

Examiner’s response:

The amended claims state that the capacitor is used to store digital value of local weights. The Examiner could not find this within the specification and rejected the independent claims under 35 U.S.C. §112 as well. Lehmann is replaced by the reference Schwartz. 'Learning electrical circuit operable to update a local weight according to an update rule' of applicant is equivalent to 'neural network’ of Schwartz.

'A digital memory arranged in parallel with the capacitor and operable to store the local weight in a digital form' of applicant is equivalent to 'Our experiments show that careful designs can reduce leakage to a level low enough that analog refresh by backing up the network with the conventional analog/digital conversion techniques and digital memory is practical if desired' of Schwartz. 'Arranged in parallel' of applicant is equivalent to 'parallel computing' of Schwartz. (**Schwartz**, abstract, p313 C1:1 through p314 C1:27) Office Action stands.

Examination Considerations

8. The claims and only the claims form the metes and bounds of the invention. "Office personnel are to give the claims their broadest reasonable interpretation in light of the supporting disclosure. *In re Morris*, 127 F.3d 1048, 1054-55, 44USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater*, 415 F.2d, 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969)" (MPEP p 2100-8, c 2, l 45-48; p 2100-9, c 1, l 1-4). The Examiner has the full latitude to interpret each claim in the broadest reasonable sense. Examiner will reference prior art using terminology familiar to one of ordinary skill in the art. Such an approach is broad in concept and can be either explicit or implicit in meaning.

9. Examiner's Notes are provided to assist the applicant to better understand the nature of the prior art, application of such prior art and, as appropriate, to further indicate other prior art that maybe applied in other office actions. Such comments are entirely consistent with the intent and sprit of compact prosecution. However, and unless otherwise stated, the Examiner's Notes are not prior art but link to prior art that one of ordinary skill in the art would find inherently appropriate.

10. Examiner's Opinion: Paragraphs 8 and 9 apply. The Examiner has full latitude to interpret each claim in the broadest reasonable sense.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Claims 43-48, 51-67, 70-88 are rejected.

Correspondence Information

13. Any inquiry concerning this information or related to the subject disclosure should be directed to the Examiner Peter Coughlan, whose telephone number is (571) 272-5990. The Examiner can be reached on Monday through Friday from 7:15 a.m. to 3:45 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor David Vincent can be reached at (571) 272-3080. Any response to this office action should be mailed to:

Commissioner of Patents and Trademarks,

Washington, D. C. 20231;

Hand delivered to:

Receptionist,

Customer Service Window,

Randolph Building,

401 Dulany Street,

Alexandria, Virginia 22313,

(located on the first floor of the south side of the Randolph Building);

or faxed to:

(571) 272-3150 (for formal communications intended for entry.)

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Peter Coughlan

9/3/2008

/David R Vincent/

Supervisory Patent Examiner, Art Unit 2129